REMARKS

This is a Response to the Office Action in the above referenced application mailed on December 3, 2004. The Office Action rejected pending claims 63-65 under 35 U.S.C. 112, first paragraph. This rejects are respectfully submitted to be in error.

Concerning the rejections in paragraph 3 of the Office Action, the Office Action states that the CONTROLLER 31 is not part of the memory card. This is incorrect. The Examiner is referred to Figure 1A that clearly shows an embodiment where the bulk storage memory 29 includes the controller 31 and the array 33 of EEPROM chips. As noted on page 7, lines 23-24, "bulk storage memory 29 of Figures 1A and 1B can be implemented on a single printed circuit card ...". That is, in this embodiment, *the card is 29, **not 33***; array 33 as well as controller 31 are part of the card.

Concerning the comment that circuit 220 of Figure 3A controls erase commands, this is correct. Figure 3A is part of the discussion of "Erase of Memory Structures" beginning at line 6 of page 8 and only highlights elements of the controller relating to the erase aspects of the present invention. Various other elements of the controller are shown in other figures relating to the discussion of these aspects: Figures 6 and 7 relate to the transfer of data; Figure 8 relates to the caching aspect. All of these elements are part of controller 31. It is unclear exactly what the Office Action is objecting to in the last part of paragraph 3, but all of the limitations of the claims are met by the various elements of the controller shown in these figures.

With respect to paragraph 4 of the Office Action, it is also unclear what the Office Action is trying to say: the first paragraph says the specification fails to disclose transmitting a chip enable signal to at least two of the memory partitions; the second sentence states that the chip enable signal is sent to selected, but ***not all***, chips; the third sentence then states a signal ***is*** sent to ***all*** chips, cites where this is done, and then quotes this in the fourth sentence. This is, the Office Action says the application fails to provide support, then recites this support in the application: consequently, it is not clear what is being asked.

If the Office Action is requiring that support be provided for "transmitting chip enable signals to at least two of the plurality of flash memory partition", as is stated in the claim, the Office Action has itself provided support for this as the global erase signal is provided to all of the partitions, which, since there are a plurality of these, it is "transmitting ... to at least two" of these.

If on the other hand the Office Action is objecting to the fact that this signal is provided to all of the chips, instead of just the selected chips, this is improper since this is not a limitation found in the claims: the claims only require that it is transmitted to at least two of the partitions, which it is. Thus, if the Office Action intends this meaning, it is requiring support for a limitation not found in the claims. (Even if this limitation were part of the claims, it should be noted that it is met by the SET ERASE EN 237 signal of Figure 3B.)

CONCLUSION

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned attorney at 415-318-1163 would be appreciated.

Respectfully submitted,

Gerald P. Parsons — March 2, 2005

Gerald P. Parsons
Reg. No. 24,486

Date

PARSONS HSUE & DE RUNTZ LLP
655 Montgomery Street, Suite 1800
San Francisco, CA 94111
(415) 318-1160 (main)
(415) 318-1163 (direct)
(415) 693-0194 (fax)